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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/673,507
Filing Date: September 30, 2003
Appellant(s): STRANG, ERIC J.

Ronald A. Rudder
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 09/02/2008 appealing from the Final Office action mailed 02/07/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

10/673,138; 10/673,467; 10/673,501; 10/673,506; and 10/673,583.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner.

- 35 USC 112 1st Paragraph Rejection of Claims 1-74 and 78-80.
- Double Patenting rejection against applications 10673138, 10673501 and 10673583.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

- **USPAT 6,802,045 Sonderman et al**
- **USPAT 6,263,255 Tan et al**
- **USPAT 5,719,796 Vincent M.C. Chen**
- **USPAT 6,812,045 Nikoonahad et al**
- **US PGPUB 20050016947 Fatke et al**
- **"Mathematic-Physical Engine: Parallel Processing for Modeling and Simulation of Physical Phenomena"; V.K.Jain et al; IEEE 1994**
- **"Heat Analysis on Insulated Metal Substrates" by Yunemura et al; IEEE 1996**

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Appellant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. **Claims 1, 8 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter) further in view U.S. Patent No. 6,263,255 issued to Tan et al (Tan hereafter).**

Regarding Claim 1

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting *process* data relating to *an actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; *Col.7 Lines 8-20*). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool *describing at least one of a basic physical or chemical attributes* (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed* during performance of actual process *(Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63,* Fig.1-3*)* using the physical model to *provide simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed* (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the first principle simulation results *obtained during the performance of the actual process* (Sonderman: Fig. 1-3 *Col.7 Lines 4-7;*

Col.3 Lines 56-63) to control the process performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; Col.7 Lines 8-20), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Arguendo, even if Sonderman and Jain do no explicitly teach said first principles simulation result being produced in a time frame shorter in time than the actual process being performed Tan teach the above limitation.

Tan teaches said first principles simulation result being produced in a time frame shorter in time than the actual process being performed as in Col.2 Lines 7-12 as:

(4) Model-based real-time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run, ensuring that product characteristics are achieved.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Tan to Sonderman to facilitate the simulation as defined in Fig.2. The motivation to combine is that both Tan and Sonderman teach performing simulation of semiconductor assembly line including the tools and the processes running on them (Tan: Col.5 Line 63-Col.6 Line 8; Sonderman: Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63, Fig.1-3).

Regarding Claim 38 (New 1/29/08)

System claim 38 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 75 (New 1/29/08)

System claim 75 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

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2. **Claims 1-21, 29-30, 32-34, 37, 38-58, 66-67, 69-71, 74, and 78-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter).**

Regarding Claim 1

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting *process* data relating to *an actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; *Col.7 Lines 8-20*). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool *describing at least one of a basic physical or chemical attributes* (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed* during performance of actual process *(Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63,* Fig.1-3*)* using the physical model to *provide simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed* (Sonderman: at least in Col.5-7), *said first principles simulation result being produced in a time frame shorter in time than the actual process being performed (Sonderman: Col.4 Lines 47-Col.5 Lines 10)*. Further, Sonderman teaches using the first principle simulation results

obtained during the performance of the actual process (Sonderman: Fig. 1-3 *Col.7 Lines 4-7; Col.3 Lines 56-63*) to control the process performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; Col.7 Lines 8-20), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process *being* performed by the semiconductor-processing tool from at least one of physical sensor (e.g. Scatterometry data, overlay data, dimensional data) and a metrology

tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator (Sonderman: at least in Fig.1-3 Col.1; Col.4-7; Col.7 Lines 8-20).

Regarding Claims 6-9

Sonderman teaches inputting process data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; Col.7 Lines 8-20). Sonderman and Jain teach inputting fundamental equations as the set of computer encoded differential equations (Sonderman: Col.9 (equations); Jain: Pg. 372 Section V Dedicated MPE, Abstract).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11-13

Sonderman teaches performing first principle simulation independent of the process performed by the semiconductor-processing tool; inputting data from to set initial & boundary condition on the first simulation model (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 14

Sonderman teaches using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Line 56 – Col.6 Line 24).

Regarding Claims 15-19

Sonderman teaches using a network of interconnected resources *inside the semiconductor manufacturing facility (Sonderman: Semiconductor tools on the factory floor – Col.9 Lines 60-65*) to perform *first principle simulation (Jain: Section III*); using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected

resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 20-21

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 29

Sonderman teaches performing a principle components analysis to determine a relationship between spatial components of said first principles simulation result for the semiconductor processing tool and a set of at least one control variable, said relationship utilized to determine a correction to said set of at least one control variable in order to affect a reduction in the magnitude of said spatial components (Sonderman: Col.5 Line 56 – Col.6 Line 23).

Regarding Claim 30

Sonderman teaches first principle simulation controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: at least in Col 4 Lines 18-31; Col.3 Lines 45-49).

Regarding Claim 32

Sonderman teaches inputting various parameters *as tool data* relating to etching, deposition etc. (Sonderman: at least in Col.5 Lines 56-67).

Regarding Claim 33

Sonderman teaches inputting physical geometric data as parameters for the equipment model where the equipment could be at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: Col.5 Lines 56-67).

Regarding Claim 34

Sonderman teaches first principles simulation result controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool (Sonderman: Col.4 Lines 48-64; Fig.1-2).

Regarding Claim 37

Sonderman teaches inspecting process results and providing input to the first principles simulation for calibration purposes (Sonderman: Col.6 Lines 14-24).

Regarding Claim 38

System claim 38 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 39

System claim 39 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claims 40-42

System claims 40-42 disclose similar limitations as claims 3-5 and are rejected for the same reasons as claims 3-5 respectively.

Regarding Claims 43-46

System claims 43-46 disclose similar limitations as claims 6-9 and are rejected for the same reasons as claims 6-9 respectively.

Regarding Claim 47

System claim 47 discloses similar limitations as claim 10 and is rejected for the same reasons as claim 10.

Regarding Claims 48-50

System claims 48-50 disclose similar limitations as claims 11-13 and are rejected for the same reasons as claims 11-13 respectively.

Regarding Claim 51

System claim 51 discloses similar limitations as claim 14 and is rejected for the same reasons as claim 14.

Regarding Claims 52-56

System claims 52-56 disclose similar limitations as claims 15-19 and are rejected for the same reasons as claims 15-19 respectively.

Regarding Claims 57-58

System claims 57-58 disclose similar limitations as claims 20–21 and are rejected for the same reasons as claims 20-21 respectively. *Change in dependency from claim 52 to claim 38 of claim 57 is noted.*

Regarding Claim 66

System claim 66 discloses similar limitations as claim 29 and is rejected for the same reasons as claim 29.

Regarding Claim 67

System claim 67 discloses similar limitations as claim 30 and is rejected for the same reasons as claim 30.

Regarding Claim 69

System claim 69 discloses similar limitations as claim 32 and is rejected for the same reasons as claim 32.

Regarding Claim 70

System claim 70 discloses similar limitations as claim 33 and is rejected for the same reasons as claim 33.

Regarding Claim 71

System claim 71 discloses similar limitations as claim 34 and is rejected for the same reasons as claim 34.

Regarding Claim 74

System claim 74 discloses similar limitations as claim 37 and is rejected for the same reasons as claim 37.

Regarding Claim 78

Article of manufacture claim 78 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claims 79-80

Jain teaches use of Navier Stokes and other known simulation solutions for solving various simulation problems as initial *condition (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).*

3. **Claims 22 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of IEEE article "Heat Analysis on Insulated Metal Substrates" by Naomi Yunemura et al (Yunemura hereafter).**

Regarding Claim 22

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above. Sonderman also teaches that the first principle simulation models the equipment conditions, thereby modeling temperature response and pressure response during various processes (Sonderman: at least in Col.5 Lines 62-67). Jain also teaches distributed and dedicated hardware implementation to solving wafer problem using computer implemented differential equations (Jain: Section III & IV).

Sonderman and Jain do not teach explicitly that such temperature and pressure modeling is done using ANSYS computer code.

Yunemura teaches that heat simulation modeling can be performed using ANSYS computer code (Yunemura: Pg. 1407 Section 1) on a silicon chip.

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Yunemura to Sonderman and Jain to create a equipment model as disclosed by Sonderman. The motivation to combine would have been that Yunemura teaches heat modeling on a silicon chip affecting the thermal conductivity (Yunemura: Pg.1407 Section 2) based on various thicknesses and Sonderman is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and affects on heat and pressure. Further, ANSYS is known in art to be used as thermal & pressure modeling tool based on finite element analysis. Motivation to combine Jain and Yunemura is that Jain as taught above indicates distributed solving of computer implemented differential equations which Yunemura solves by ANSYS modeling, thereby facilitating in implementation of Jain's teachings.

Regarding Claim 59

System claim 59 discloses similar limitations as claim 22 and is rejected for the same reasons as claim 22.

4. **Claims 23-28 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter).**

Regarding Claims 23-25

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above.

Sonderman and Jain does not explicitly teach close fitting the solution of the first principle simulation run to thereby set initial conditions for cells in the first principle simulation; selecting close fitting solutions from a library based on convergence.

Chen teaches close fitting the solution of the first principle simulation run to thereby set initial conditions for cells in the first principle simulation; selecting close fitting solutions from a library based on convergence (Chen: at least in Col.5 Lines 38 – Col.6 Line 25; Fig 3A-B).

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Chen to Sonderman and Jain. The motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23).

Regarding Claim 26

Chen teaches that the close-fitting solution library existing on a network of computers connected to semiconductor-processing tool (Chen: Fig.2; Col.4 Line 55 –Col.6 Line 19).

Regarding Claims 27-28

Chen teaches calculating solution to the first principle simulation by choosing a coarse grid for solution to the first principle simulation (Chen: at least in Col.6 Line 44-Col.7 Line 14) as user defined parameters; further, subsequent solutions by setting the initial conditions to fine grid are made though Gaussian distribution and actual inline data (Chen: at least in Col.6 Line 46-51).

Regarding Claims 60-62

System claims 60-62 disclose similar limitations as claims 23-35 and are rejected for the same reasons as claims 23-25 respectively.

Regarding Claim 63

System claim 63 discloses similar limitations as claim 26 and is rejected for the same reasons as claim 26.

Regarding Claims 64-65

System claims 64-65 disclose similar limitations as claims 27-28 and are rejected for the same reasons as claims 27-28 respectively.

5. **Claims 31, 36, 68 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine:**

parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), in view of U.S. Patent No. 6,812,045 issued to Mehrdad Nikoonahad (Nikoonahad hereafter).

Regarding Claim 31

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above. Sonderman provides examples of the processing tool as etch and photolithography tools (Col.4 Lines 26-31) but does not explicitly disclose chemical vapor and physical vapor deposition system.

Nikoonahad teaches deposition tools to include chemical vapor and physical vapor deposition system (Nikoonahad: Col.24 Lines 3-49).

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Nikoonahad to Sonderman and Jain. The motivation to combine would have been that Nikoonahad and Sonderman are analogous art and both are modeling the semiconductor processing and providing feedback to the semiconductor processing tool (Sonderman: Abstract; Nikoonahad: Col.3; Col.93 Lines 20-35).

Regarding Claim 36

Nikoonahad teaches plurality of computing (as processor)/ storage (as memory) devices connected over network to exchange information between a plurality of computing/storage devices including at least one of model solver parameters, solution status to the first principles simulation, model solutions to the first principles

simulation, and solution convergence history for said model solutions (Nikoonahad: Col.3 Lines 15-44; Col.68, Lines 41-59).

Regarding Claim 68

System claim 68 discloses similar limitations as claim 31 and is rejected for the same reasons as claim 31.

Regarding Claim 73

System claim 73 discloses similar limitations as claim 36 and is rejected for the same reasons as claim 36.

6. **Claims 35 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Application 10/472,436 filed by David Fatke et al. US PGPUB 20050016947 (Fatke hereafter).**

Regarding Claim 35

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above.

Sonderman and Jain do not teach step of controlling by utilizing at least on of non-linear optimization and multivariate analysis to derive the control model for the process control.

Fatke teaches utilizing at least on of non-linear optimization and multivariate analysis to derive the control model for the process control (Fatke: [0011][0012][0035][0050]-[0058][0021]). Fatke uses the partial least square (PLS) model to perform multivariate analysis ([0050] to derive the control model for the process control and provide output to the semiconductor-processing tool ([0021]).

Further, Fatke teaches that the nonlinear optimization is known in the art for creating such models ([0012]).

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Fatke to Sonderman and Jain. The motivation to combine would have been that Fatke and Sonderman are analogous art and Fatke creates a model form the determining the endpoint of the etching in an etch reactor (Fatke: Abstract/Summary), thereby creating a equipment model and the process model for etching, which can be applied to Sonderman.

Regarding Claim 72

System claim 72 discloses similar limitations as claim 35 and is rejected for the same reasons as claim 35.

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(10) Response to Argument

A. Regarding the 35 USC 112 1st Paragraph Rejection of Claims 1-74 and 78-80

Although examiner has withdrawn the rejection under this statue, and the claims are given the broadest reasonable interpretation consistent with the specification, the arguments provided for claim 1, 38 and 78 limitations are more specific than the limitations. Specifically, the limitation

> "… performing first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, **said first principles simulation result being produced in a time frame shorter in time than the actual process being performed**, and"

as argued by the appellant on Pg.13-14 of appeal brief, states reasons *why the time frame is shorter*, are more specific than claimed above. Further as shown by Fig.3 on same page the simulation module 302 is not claimed to be the part of the tool 102.

B. Regarding the 35 USC 103 Rejection of Claims 1 and 8 over Sonderman et al Jain et al and Tan et al

(Argument 1) Appellant has argued in Remarks Pg.16:

> The plain reading of this section of Sonderman et al is that the system 100 then (e.g., at time T1) optimizes the simulation for each silicon wafer, Si to be processed (e.g., later at time T2). In other words, the simulation results of Sonderman et al produce a new control input for each silicon wafer to be processed. Thus, Appellant respectfully submits that Sonderman et al teach performing a simulation result for a process to be performed before performance of the actual process, and do not teach the claimed performing first principles simulation for the actual process being performed during performance of the actual process.

(Response 1) Appellant above cites Sonderman Col.9 Lines 45-61 Stating:

FIG. **10** illustrates a chart that represents the percentage effectiveness of the each process performed on each silicon wafer (S_1, S_2 . . . S_i). Some processes P_i can be more effective than others in reaching a desired performance goal. The electrical parameter Y, relating to the processed silicon wafer S_i, is generally a multi-variant function of S_i process steps, as illustrated by Equation 2.

$$Y=f(S_1, S_2, S_3 \ldots S_i) \quad \text{Equation 2}$$

The system **100** then optimizes the simulation (described above) to find more optimal process target (T_i) for each silicon wafer, S_i, to be processed. These target values are then used to generate new control inputs, X_{Ti}, on the line **805** to control a subsequent process of a silicon wafer S_i. The new control inputs, X_{Ti}, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool **120** operating scenarios, and the like.

Here examiner would like to emphasize that new control inputs X_{Ti} are generated to control the "subsequent [part of the] process" (applicable to same process as inputs are *pertinent* to same process only - e.g. metal deposition on substrate where inputs may specify to deposit more metal) on the silicon wafer S_i.

Arguendo, If Sonderman was intending to use the inputs for the next wafer he would have stated for silicon wafer S_{i+1}, with emphasis on subscript i+1.Therefore as the limitation "***for the actual process being performed during performance of the actual process***", is performed during the processing of silicon wafer (See Sonderman Fig.1).

(Argument 2) Appellant has argued in Remarks Pg.16-18:

> "Other sections of Sonderman et al support Appellant's position on this matter that the **simulation results in Sonderman et al are made prior to controlling a subsequent process**. For instance, Figure 4 of Sonderman et al (reproduced below) shows that the simulation results are produced ahead of performing a process and **thus have to be based on historical data**.
>
> … With reference to **Figure 4, Sonderman et al disclose at col. 6, lines 24-47**:…
>
> Appellant respectfully points out that this description in Sonderman et al is a description of a **feedback loop** as Sonderman et al describe just below that portion which the examiner emphasized. Feedback modification is by definition the control of future wafers based on what has already occurred to a previous wafer. Hence, this section supports rather than refutes Appellant's position on this matter."

(Response 2) Examiner respectfully disagrees as Sonderman Col.4 Lines 65-Col.5 Lines 10 states:

65 Furthermore, the simulation environment **210** can be used for feedback modification of control parameters invoked by the process control environment **180**. For example, the

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manufacturing environment **170** can send metrology data results into the simulation environment **210**. The simulation environment **210** can then use the metrology data results and perform various tests and calculations to provide more accurate, modified control parameters to the process control environment **180**. A feedback loop in then completed when the process control environment **180** sends the modified or adjusted process control parameters to the manufacturing environment **170** for further processing of semiconductor wafers.

As clearly seen, the control parameter from the process control environment are first fed into the simulation environment, and then the post simulation output, having modified control parameters, is used to control the process control environment. Thus the results are not based on the historical data for another run, but are from the same run, where the input from *the* process control environment provided to

simulation tool is used to generate modified control parameter for *the* process control environment.

Appellant recital of Sonderman Col.6 and Fig.4 are noted, however they are part of the picture shown in the Col.4 teaching above of the Sonderman. Appellant is picking in the chicken & egg situation, which one came first. As stated the process control is a feedback process (See Sonderman Fig.1 and 8) where the metrology data is used as input to simulation tool (Fig.1) and output as shown above is applied to subsequent part of the process.

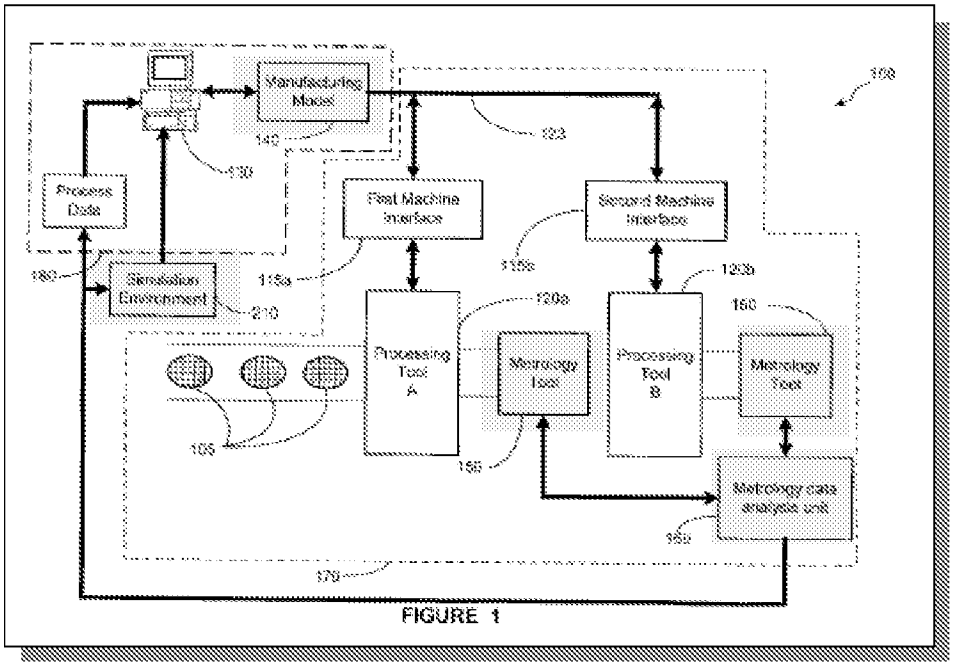


FIGURE 1

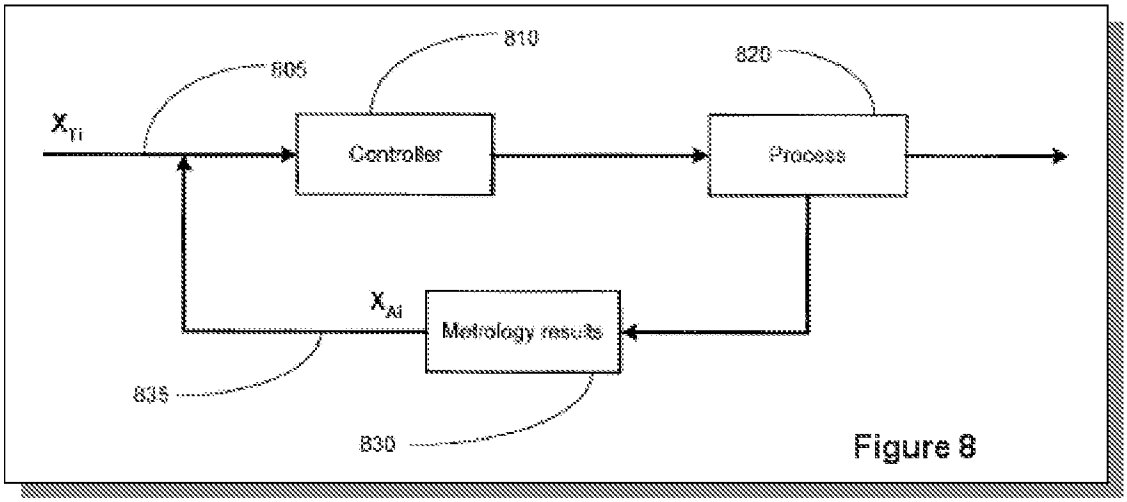


Figure 8

(Argument 3) Appellant has argued in Remarks Pg.18:

> Accordingly, Appellant respectfully submits that Sonderman et al do not disclose and indeed ***teach away*** from the present invention where data input from an actual process being performed is used for producing a first principles simulation result, **[1]** which is produced for the actual process being performed during performance of the actual process for control of the actual process. **[2]**

(Response 3) Appellant has not presented any rationale why Sonderman teaches away. As shown argument [1] is taught by Sonderman in Col.4 Line 65-Col.5 Line 10. As shown above argument [2] is taught by Sonderman in Col.9 Lines 40-51 (See response 1).

(Argument 4) Appellant has argued in Remarks Pg.19:

> The deficiencies in Sonderman et al are not overcome by Jain et al. The Office Action in rejecting the present claims supplements the teachings of Sonderman et al with the teachings of Jain et al for their teaching of computer encoded differential equations in a mathematical physical engine (MPE) which can be applied to wafer processing. See Office Action, page 16. Jain et al describe at pages 372-373 that:…
> Thus, as emphasized above, the proposed development work in Jain requires the development of ***futuristic*** computational equipment which one of ordinary skill in the art would be reluctant to implement or utilize for the rigorous standards needed in semiconductor manufacturing.

(Response 4) Teaching of Jain, in defining the MPE as first principle simulation model, are adequate in terms of modeling the semiconductor environment. Further,

appellants own specification does not disclose any more details than present in Jain. (Please see Specification [0035]-[0036]).

(Argument 5) Appellant has argued in Remarks Pg.20-23:

> Arguments pertaining to Tan and Kee references.

(Response 5) Although, Tan and Kee references are not presented as grounds of rejection in this case and arguments pertaining to them are not relevant to instant rejection, Examiner notes reference being made to APC control (In Tan), which is also present in Sonderman. It is common knowledge in the art of semiconductor processing that Advanced Process Control (APC) is a real-time system which provides process control to semiconductor processing tool. As seen from Sonderman APC control integrates the simulation tool (Sonderman: Col.9 Lines 57-Col.10 Line 20) therefore by sheer nature, the simulation tool also need to be real time and *not run sequentially* as suggested by appellant in previous arguments. Sonderman does not suggest any historical database as suggested in Tan.

(Argument 6) Appellant has argued in Remarks Pg.23:

> The examiner in the final Office Action did not apply but rather noted the IEEE 1990 paper by Su-shing Chen, "AEMPES: An expert system for in-situ diagnostics and process monitoring," hereinafter referred to as AEMPS, as evidence that the newly added limitation (said first principles simulation result being produced in a time frame shorter in time than the actual process being performed) is known in the art. Yet, AEMPS describes the use of simulation in neural network environment used to "leam processes and the equipment model." See page 120, section 4. AEMPS describes in section 4 that "a rule-based expert system provides human interfaces and high-level decision support." Accordingly, AEMPS does not describe a first principles simulation result, but rather describes a neural network leaming-based simulation…

(Response 6) First AEMPES was not used in the rejection. Secondly, even if used appellant is performing piecemeal analysis of AEMPES as the first simulation model

is taught by Jain. Arguments pertaining to AEMPES are withdrawn and not applicable to instant invention.

(Argument 7) Appellant has argued in Remarks Pg.24-25:

> More importantly, numbered paragraphs [0004] and [005] indicate at most that the times for a large number of simulations typically done in the tool design stage are comparable to wafer or wafer cassette processing times. There is no statement here regarding how long the times would be for a process control simulation. Further, numbered paragraphs [0004] and [005] indicate that, at the time of the invention, there were serious impediments which would mean that it would not be possible, prior to the invention, to produce a first

(Response 7) As seen from the cited paragraphs [0004]:

> "…Indeed, the present inventors have recognized that a large number of simulations typically done in the tool design stage can presently be **run in times comparable to wafer or wafer cassette processing times**…"

Clearly refers to the time period of the simulation as comparable to the wafer processing times. Therefore the statement [1] above is contradictory to what specification background states.

(Argument 8) Appellant has argued in Remarks Pg.25:

> Hence, Tan et al, Jain et al, Kee et al, AEMPES, and the background section of the specification all discredit any suggestion that the examiner may have read from the disclosure of Sonderman et al for real-time simulation and control of an actual process being performed.

(Response 8) Besides being conclusory, the statement above contradicts what is known in the art as real time control - i.e. *Advanced Process Control (APC) for the semiconductor processing tools. Sonderman (Col.9 Lines 57-Col.10 Line 20) clearly shows integration of the simulation tool with APC and by definition APC is real time, it implies real time simulation as well.* Further Appellant has never claimed "real-time simulation and control" as argued against Sonderman & Jain and implied from Tan et al, Jain et al, Kee et al, & AEMPES.

(Argument 9) Appellant has argued in Remarks Pg.26:

> In the present situation, the claimed elements worked together in an unexpected and fruitful manner as compared to the prior art. For example, since in Sonderman et al there are new control inputs for each subsequent wafer, **[1]** one can not compensate for real time excursions from the existing model occurring while the wafer is being processed. In other words, the historically lengthy time for generation of a first principles model simulation would mean that, in Sonderman et al, one is prevented from realizing a real time process control based on a first principles simulation during the actual process being performed. **[2]** Meanwhile, the claimed processes and systems (by producing a first principles simulation result in a time frame shorter in time than the actual process being performed) permits accurate control of the process even if the system being controlled deviates from its historical behavior.

(Response 9) As per [1], this allegation is unsubstantiated and rebutted above in Response 1. As per [2], appellant is reading deficiencies presented in older reference Tan (dated 2001) and Kee (dated 1996) into more current Sonderman (dated 2004) without providing support for the allegation in [2] that Sonderman is not able to overcome those deficiencies. Further, it seems appellant is presenting argument against validity and operability of Sonderman's teaching. Under 35 USC 282, a patent is presumed valid for it teachings.

C & D. Regarding the 35 USC 103 Rejection of Claims 1-21, 29-30, 32-34, 37, 38-58, 66-67, 69-71, and 74 over Sonderman et al and Jain et al

No new arguments are presented by appellant under this section. Please see section B above as response for section C above.

As for Section D:

(Argument 10) Appellant has argued in Remarks Pg.27-28:

> Jain et al in section II describe a virtual mathematical physical engine (MPE) or dedicated MPE "consisting of hundreds or thousands of processors. Jain et al in section 11I describe a parallel architecture used in the MPE described therein. Section IV ofJain et al more specifically describes a networking of computational resources across the country, which it describes as "essential in the implementation of the virtual MPE." Accordingly, Jain et al in teaching the essential use of networking across the country (probably for the reason of having access to hundreds or thousands of processors) teach away from Claim 15, where there is a network of

> interconnected ***resources inside a semiconductor device manufacturing facility*** that is used to perform the first principles simulation.

(Response 10) Appellant is performing piecemeal analysis. Teaching of Sonderman is used to show exemplary simulation engine coupled to the manufacturing facility. Jain does not teach away from such a facility but utilizes the advances in computing to speed up and enhance the simulation by distributing it (Jain: See Fig.2 on a same chip having multiple PE's with interconnect. Another example on Fig.4) thereby teaching interconnect-resource limitation in the claims 15-19. Appellant has merely alleged teaching away without providing any rationale.

E. Regarding the 35 USC 103 Rejection of Claims 79 and 80 over Sonderman et al and Jain et al

(Argument 11) Appellant has argued in Remarks Pg.28-29:

> Claim 79 defines that the performing a first principles simulation includes providing for the first principles simulation a reuse of known solutions as initial conditions for the first principles simulation. The Office Action notes that "Jain teaches use of Navier Stokes and other known simulation solutions" and cites pp. 367-368 of Jain et al. However, the Navier Stokes equation on page 367 of Jain et al is a fluid flow equation which needs boundary conditions and which need s to be solved in order to produce a solution. The Navier Stokes equation on page 367 of Jain et al does not represent a solution, much less the reuse of known solutions as initial conditions for the first principles simulation. Appellant's inspection of the remainder of Jain et al finds no disclosure of the reuse of known solutions as initial conditions for the first principles simulation.

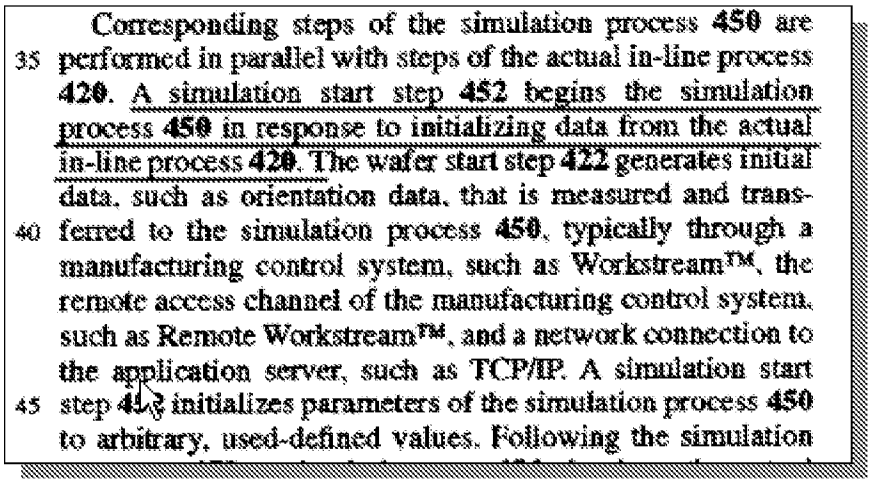
(Response 11) Claim 79 does not require “boundary condition” limitation as alleged by appellant. Arguendo even if it did, Jain teaches using Navier Stokes equation and one of ordinary skill in the art of fluid flow simulation would know that such a boundary would be necessary to implement and come to conclusion as presented in Jain. The reuse of the solution would be obvious from Sonderman *Col.7 Lines 8-20.*

G. Regarding the 35 U.S.C. § 103 Rejection of Claim 23-28 and 60-65 over Sonderman et al and Jain et al and Chen

(Argument 12) Appellant has argued in Remarks Pg.30:

> Specifically, there is no disclosure in Chen of 1) setting initial conditions in a first principles simulation, or 2) setting the initial conditions for cells in a first principles simulation. Thus, a combination of Chen with Sonderman et al and Jain et al would not yield these claim features.

(Response 12) Examiner respectfully disagrees as the simulation is initialized as shown in Chen Col.6 Lines 35-46 at least.



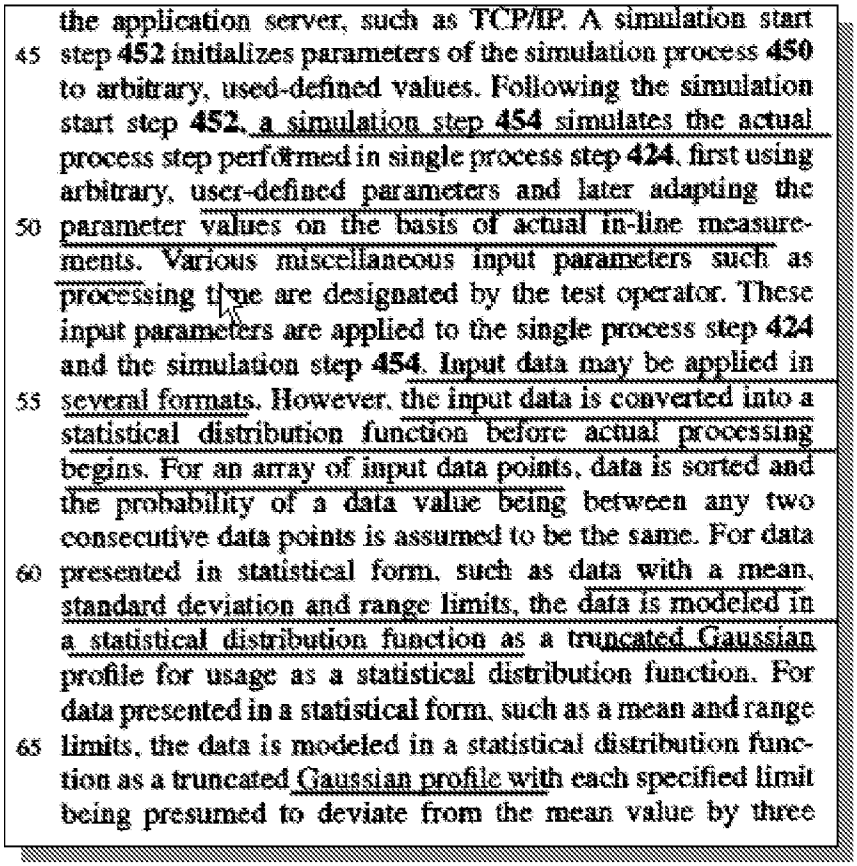
Corresponding steps of the simulation process **450** are performed in parallel with steps of the actual in-line process **420**. A simulation start step **452** begins the simulation process **450** in response to initializing data from the actual in-line process **420**. The wafer start step **422** generates initial data, such as orientation data, that is measured and transferred to the simulation process **450**, typically through a manufacturing control system, such as Workstream™, the remote access channel of the manufacturing control system, such as Remote Workstream™, and a network connection to the application server, such as TCP/IP. A simulation start step **452** initializes parameters of the simulation process **450** to arbitrary, used-defined values. Following the simulation

Therefore appellant's arguments are not persuasive.

(Argument 13) Appellant has argued in Remarks Pg.30:

> Furthermore, there is no disclosure in Chen for the features defined in Claims 27-28 and 64-65 regarding choosing a coarse grid for a solution of the first principles simulation (Claims 27 and 64) and then using the solution for coarse grid in a fine grid simulation (Claims 28 and 65).

(Response 13) Chen teaches these limitations in Col.6 Line 46-51:



the application server, such as TCP/IP. A simulation start step **452** initializes parameters of the simulation process **450** to arbitrary, used-defined values. Following the simulation start step **452**, a simulation step **454** simulates the actual process step performed in single process step **424**, first using arbitrary, user-defined parameters and later adapting the parameter values on the basis of actual in-line measurements. Various miscellaneous input parameters such as processing time are designated by the test operator. These input parameters are applied to the single process step **424** and the simulation step **454**. Input data may be applied in several formats. However, the input data is converted into a statistical distribution function before actual processing begins. For an array of input data points, data is sorted and the probability of a data value being between any two consecutive data points is assumed to be the same. For data presented in statistical form, such as data with a mean, standard deviation and range limits, the data is modeled in a statistical distribution function as a truncated Gaussian profile for usage as a statistical distribution function. For data presented in a statistical form, such as a mean and range limits, the data is modeled in a statistical distribution function as a truncated Gaussian profile with each specified limit being presumed to deviate from the mean value by three

Here the input is converted to several formats with ranges/limits and statistical distributions mapped to grids of the claim. Further the coarse grid would be the user defined initial input and fine grid would be mapped to the actual in-line measurements.

H. Regarding the 35 U.S.C. § 103 Rejection of Claims 31, 36, 68, and 73 over Sonderman et al and Jain et al and Nikoonahad

(Argument 14) Appellant has argued in Remarks Pg.31:

> The Office Action applied Nikoonahad to overcome the deficiencies of Sonderman et al and Jain et al regarding the features of Claims 31, 36, 68, and 73. Yet, the examiner's position as to why it would have been obvious to combine Nikoonahad to Sonderman et al and Jain et al is merely a statement of the teachings being analogous art and both concerning modeling. Yet, KSR requires an articulated rationale as to why the claimed features are obvious and indicates that conclusory statements are not sufficient.

(Response 14) Examiner did provide a rationale stating:

> It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Nikoonahad to Sonderman and Jain. The motivation to combine would have been that Nikoonahad and Sonderman are analogous art and both are modeling the semiconductor processing and providing feedback to the semiconductor processing tool (Sonderman: Abstract; Nikoonahad: Col.3; Col.93 Lines 20-35).

Under KSR, Nikoonahad is a known work in the field of endeavor which may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art. In this case the Nikoonahad teaches modeling and simulation (Fig.10 at least) in conjunction with semiconductor fabrication process.

I. Regarding the 35 U.S.C. § 103 Rejection of Claims 35 and 72 over Sonderman et al and Fatke

(Argument 15) Appellant has argued in Remarks Pg.31:

> The Office Action applied Fatke et al to overcome the deficiencies of Sonderman et al regarding the features of Claims 35 and 72. Yet, the examiner's position as to why it would have been obvious to combine Fatke et al with Sonderman et al is merely a statement that the teachings are analogous art and the asserted existence in Fatke et al of one of the claimed elements, which the Office Action asserts can be applied to Sonderman et al.

(Response 15) Examiner had stated in the motivation to combine:

> It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Fatke to Sonderman and Jain. The motivation to combine would have been that Fatke and Sonderman are analogous art and Fatke creates a model form the determining the endpoint of the etching in an etch reactor (Fatke: Abstract/Summary), thereby creating a equipment model and the process model for etching, which can be applied to Sonderman.

Fatke, as can be clearly seen again, is a known work in the field of semiconductor process modeling, which may prompt variations as per KSR and would be obvious to combine it with Sonderman and Jain. Here the variation is the variation in the model of plasma etch process (Fig.4 & 6).

J. Regarding the Double Patenting Rejections

Double patenting rejection is withdrawn in view of the terminal disclaimer filed by appellant.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Akash Saxena/

Examiner, Art Unit 2128

Conferees:

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128

/Paul L Rodriguez/

Supervisory Patent Examiner, Art Unit 2123